REMARKS

Claims 1-4, 8-9, and 29-34 are pending. No claims have been amended.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1-4, 8-9, and 29-34 under 35 U.S.C. § 103(a) as being obvious over Xiang et al. (US Patent 6,586,808) in view of Long et al (6,744,101).

Applicant respectfully disagrees with the Examiner's position that the rejected claims are obvious over Xiang in view of Long. First, it is Applicant's position that the Xiang and Long references, even if combined, lack features of Applicant's claimed device *as a whole.* Second, Applicant understands the Xiang reference to teach away from Applicant's invention *as a whole* and therefore a combination with Xiang does not render Applicant's invention obvious.

Applicant's independent claim 1 specifies an *n-type* (NMOS) transistors with a gate electrode having a *central* portion with a work function *which is higher than* the work functions of *a pair of sidewall* portions. Thus, the Applicant's *n-type* transistor has a gate metal electrode segmented into *low/high/low* work functions. As previously noted in the record, the Xiang reference only discloses an *n-type* device having a segmented gate metal electrode with an *oppositely* configured work function differential: *high/low/high.* (Xiang, Col 4, lines 29-32). It is Applicant's position the Long reference cited by the Examiner fails to cure this deficiency in Xiang because Long merely discloses an *n-type* transistor having a three segment gate electrode wherein the work function varies *low/medium/high* or *high/medium/low* from the source to the drain (Long, Col 5, lines 49-50 and 57-58). Applicant Therefore, Applicant understands the Long reference to disclose that *either* the source side or the drain side of the gate electrode may have a *lower* work function than the central portion, but not *both.* In contrast, Applicant's claimed n-type device with a *low/high/low* work function gate electrode feature has *both* sidewall portions with a work function that is lower. Because nowhere in Long is an *n-type* device disclosed having the feature of *both* sidewall portions with a *lower* work function than the central portion, the deficiency in Xiang remains. Thus, it is Applicant's understanding that the combination of

Xiang and Long still lacks the features as a whole of the n-type devices in claim 1. Applicant offers an analogous argument for claim 29, referring to the claimed *p-type* devices having *high/low/high* work functions. Applicant's claimed p-type devices are again opposite to Xiang's low/high/low p-type device (Xiang, Col 4, lines 32-35) and the high/low/high feature is again not disclosed in Long (Col 5, line 60 to Col 6, line 10).

Additionally, it is Applicant's position that the Xiang reference clearly teaches away from Applicant's invention as a whole. Applicant respectfully disagrees with the Examiner's position that Xiang merely teaches the "concept of forming a gate electrode having a central portion and sidewall portions, wherein the two portions have different work functions." Rather, it is Applicant's position that Xiang teaches the concept of forming a gate electrode with a work function arrangement having a *specific relationship to the conductivity type* of the device.

Applicant's *n-type* (NMOS) transistors have a *low/high/low* work function gate electrode. In contrast, Xiang's *n-type* transistors have a *high/low/high* work function gate electrode. Xiang's disclosed work function arrangement has the opposite relationship to device conductivity type Applicant taught and claimed. Applicant notes Xiang was concerned with short channel effects (SCE) (Xiang column 1, lines 35-48) and states, "the material used for the lateral gate portions is selected such that the device threshold near the source and the drain is higher than the device threshold (expressed in absolute value) in a middle region of the channel." (Xiang, col 3, lines 36-40). Thus, the work function differential between the central and sidewall portions as it is *critically dependent* on the conductivity type of the transistor and is an *essential aspect* of Xiang's disclosure. Accordingly, Applicant understands the Xiang reference to indicate Applicant's n-type device combined with a low/high/low work function gate electrode would have *degraded*, not *improved* SCE. Thus, it is Applicant's position that Xiang clearly teaches away from Applicant's claimed n-type devices *as a whole*. Applicant further notes that Xiang is not merely silent on a low/high/low work function arrangement, but instead clearly states such an arrangement is *only* used for a *p-type* transistor. (Xiang Col 4, lines 29-35). Applicant respectfully offers this as additional evidence that Xiang teaches away from Applicant's n-type devices of claim 1 and p-type devices of claim 29.

Applicant also respectfully disagrees with the Examiner's statement that the Long reference discloses "the sidewall portions may have either a higher work function or a lower work function." Instead, Applicant understands Long to show that a device can have a gate electrode where the work function might *either monotonically decrease* (high/medium/low) or *monotonically increase* (low/medium/high) from the source to the drain. (Long, Col. 5, line 45 to Col 6, line 10). Applicant therefore fails to find any disclosure in Long that would provide a motivation to modify the Long device to have *both* the sidewall portions to be made to have lower work functions than the central portion (low/high/low) as in Applicant's n-type device of claim 1. Instead, Applicant considers the Long reference to merely provide motivation for a three segmented gate electrode having a monotonically graduated work function for either a n-type or p-type device. Similarly, Applicant notes the same is true for Applicant's "high/low/high" p-type device of claim 29.

Applicant wishes to emphasize the significance of Xiang disclosing devices of a conductivity type *complementary* to that of Applicant's taught devices. Applicant respectfully submits to the Examiner that Xiang's stated goal and disclosed devices teach away from Applicant's claimed devices *as a whole*. Because the Long reference fails to provide motivation to modify either Long or Xiang to accomplish the *exact opposite* of Xiang's instruction, Applicant's considers the claimed devices to be nonobvious over the cited references.

On this basis, Applicant' respectfully requests the Examiner to remove the 35 U.S.C. §103(a) rejection of claims 1-4, 8-9, and 29-34.

Applicant respectfully submits that in view of the arguments set forth herein, the applicable rejections have been overcome and the present application is in condition for allowance.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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